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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/779,424	02/08/2001	Paras A. Shah	COMP:0187/FLE (P00-3008)	5601

7590 04/13/2004

INTELLECTUAL PROPERTY ADMINISTRATION
LEGAL DEPARTMENT, M/S 35
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EXAMINER	
KNOLL, CLIFFORD H	

ART UNIT	PAPER NUMBER
2112	7

DATE MAILED: 04/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No	Applicant(s)	
	09/779,424	SHAH, PARAS A.	
	Examiner	Art Unit	
	Clifford H Knoll	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is responsive to communication filed 2/5/04. Claims 1-30 are currently pending.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 102

Claims 1-15, 20-23, 25-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Kelly (US 5996036).

Regarding claims 1, 6, 9, and 25, Kelly discloses methods and system means for temporarily storing transaction entries (e.g., col.9, lines 30-36); selecting one of the plurality of temporarily stored entries and enqueuing the selected one (e.g., col.9, lines 44-46).

Regarding claims 2, 7, 10, and 26, Kelly also discloses storing in a bank of registers (e.g., col.8, lines 15-21).

Regarding claim 3, Kelly also discloses storing entries simultaneously (e.g., col.9, lines 31-36).

Regarding claims 4, 8, 11, and 27, Kelly also discloses determining whether a posted write is present and enqueuing the posted write, if the posted write transaction is not present then determining whether a read completion is present and enqueuing the

read completion (e.g., col.14, lines 12-15), if the read completion transaction is not present (e.g., col.17, lines 40-46) determining whether a delayed/split transaction entry is present and enqueuing the delayed/split transaction entry (e.g., col.20, lines 12-19).

Regarding claim 5, Kelly also discloses enqueuing each entry into the transaction order queue one at a time during successive clock cycles (e.g., col.9, lines 7-12).

Regarding claim 12, Kelly discloses temporary storage to store a plurality of transaction entries (e.g., col.9, lines 30-36), selecting and ordering the plurality of entries (e.g., col.9, lines 44-46).

Regarding claim 13, Kelly also discloses storing in a bank of registers (e.g., col.8, lines 15-21).

Regarding claim 14, Kelly also discloses determining whether a posted write is present and enqueuing the posted write, if the posted write transaction is not present then determining whether a read completion is present and enqueuing the read completion (e.g., col.14, lines 12-15), if the read completion transaction is not present (e.g., col.17, lines 40-46) determining whether a delayed/split transaction entry is present and enqueuing the delayed/split transaction entry (e.g., col.20, lines 12-19).

Regarding claim 15, Kelly also discloses enqueuing each entry into the transaction order queue one at a time during successive clock cycles (e.g., col.9, lines 7-12).

Regarding claim 20, Kelly discloses determining whether a posted write is present and enqueuing the posted write, if the posted write transaction is not present then determining whether a read completion is present and enqueuing the read

completion (e.g., col.14, lines 12-15), if the read completion transaction is not present (e.g., col.17, lines 40-46) determining whether a delayed/split transaction entry is present and enqueuing the delayed/split transaction entry (e.g., col.20, lines 12-19).

Regarding claim 21, Kelly also discloses enqueuing one transaction entry per clock cycle (e.g., col.9, lines 7-12).

Regarding claim 22, Kelly discloses a processor and memory, and a transaction order queue circuit configured to process transactions from the memory device the transaction order queue circuit being adapted to encode a plurality of simultaneous transaction entries (e.g., col.9, lines 44-46).

Regarding claim 23, Kelly also discloses determining whether a posted write is present and enqueuing the posted write, if the posted write transaction is not present then determining whether a read completion is present and enqueuing the read completion (e.g., col.14, lines 12-15), if the read completion transaction is not present (e.g., col.17, lines 40-46) determining whether a delayed/split transaction entry is present and enqueuing the delayed/split transaction entry (e.g., col.20, lines 12-19).

Regarding claim 28, Kelly discloses methods and system means for temporarily storing transaction entries (e.g., col.9, lines 30-36), selecting one of the plurality of temporarily stored entries and transmitting according to priority (e.g., col.8, line 62 – col.9, line 2).

Regarding claim 29, Kelly also discloses entries are stored simultaneously in a bank of registers (e.g., col.9, lines 44-46).

Regarding claim 30, Kelly also discloses determining whether a posted write is present and enqueuing the posted write, if the posted write transaction is not present then determining whether a read completion is present and enqueuing the read completion (e.g., col.14, lines 12-15), if the read completion transaction is not present (e.g., col.17, lines 40-46) determining whether a delayed/split transaction entry is present and enqueuing the delayed/split transaction entry (e.g., col.20, lines 12-19).

Thus are claims 1-15, 20-23, 25-30 rejected.

Claim Rejections - 35 USC § 103

Claims 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kelly in view widely known enhancement of the PCI standard, as evidenced by of Willenborg (US 6477610).

Regarding claim 16, Kelly discloses a first logic device, and a plurality of registers configured to receive a plurality of transaction entries as ordered by the first logic device (e.g., col.8, line 62 – col.9, line 2); a second logic device to receive the entries and programmed to select transactions according to PCI or PCI-like specifications (e.g., col.5, lines 52-55). Kelly does not expressly mention the PCI-X bus; however Examiner takes Official Notice that this PCI enhancement specification is broadly known in the industry as exemplified by Willenborg. Willenborg discloses the PCI-X specification as the enhanced version of the PCI specification (e.g., col. 1, lines 54-61).

It would have been obvious to combine Kelly with the PCI-X, because PCI-X is commonly known as an enhancement of the PCI standard. Therefore it would have been obvious, at the time the invention was made, for a person of ordinary skill in the art to combine Kelly with an obvious standard enhancement.

Regarding claim 17, Kelly also discloses receiving transaction entries from an input source (e.g., col.9, lines 30-36).

Regarding claim 18, Kelly also discloses storing in a bank of registers (e.g., col.8, lines 15-21).

Regarding claim 19, Kelly also discloses selecting a single entry to send to the transaction order queue (e.g., col.9, lines 44-46).

Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kelly in view of Willenborg (US 6477610).

Regarding claim 24, Kelly discloses a processor and memory, and a transaction order queue circuit configured to process transactions from the memory device the transaction order queue circuit being adapted to encode a plurality of simultaneous transaction entries (e.g., col.9, lines 44-46). Kelly does not expressly mention the computer having network capabilities; however, Willenborg discloses network capabilities (e.g., col. 1, lines 54-61). It would have been obvious to combine Kelly with Willenborg, because Willenborg teaches the widely known and advantageous use of network capabilities in a PCI system such as Kelly. Therefore it would have been

obvious, at the time the invention was made, for a person of ordinary skill in the art to combine Kelly with Willenborg.

Response to Arguments

Applicant's arguments on pages 19-20, with respect to rejection under 35 USC 103 of claims 16-19 and 24, have been fully considered and are persuasive. The rejection of these claims under 35 USC 103, incorrectly using Shah as a teaching reference has been withdrawn. A new rejection of these claims is made above.

Applicant's arguments on pages 14-18, with respect to 35 USC 102 rejection using Kelly, have been fully considered but they are not persuasive.

Applicant states that citation of Kelly was not specific enough to make an accurate interpretation. While Applicant is required to consider the prior art in its entirety, the issue is moot inasmuch as this Office Action will be made non-final for the purpose of introducing a new ground of rejection for claims 16-19 and 24. The following response to Applicant's arguments should serve to clarify interpretation of Kelly. Applicant argues that passages cited in Kelly "is the address bus arbiter state machine" (p. 16); this is indeed the correct passage. Applicant argues that "the Kelly reference cannot possibly disclose '*enqueuing* the selected one of the plurality of the temporarily stored transaction entries *in the transaction order queue*'" (p. 16, emphasis original). Applicant argues similarly on subsequent pages 17-18: "Kelly reference fails to disclose enqueuing (or delivering entries to) a transaction order queue" (p. 17) and "[f]or reasons very similar to those discussed above with regard to claims 1, 6, 9, and 25, independent

claims 12, 22, and 28 are also clearly not anticipated by the Kelly reference. Since the Kelly reference does not disclose a transaction order queue, it cannot disclose 'logic adapted for selecting and ordering the plurality of transaction entries in the transaction order queue,' as recited in claim 12" (p. 18).

However the transaction order queue as it is claimed is anticipated by Kelly's arbiter. In the claimed invention, a single entry is selected from the temporary queue and then enqueued. It is the obligation of the Examiner to assume the broadest reasonable interpretation of the claimed invention. For the purposes of examination, a *queue with a single entry as it is currently recited must be considered equivalent to a buffer*. This is consonant with a selection of *a single entry* and the *enqueuing* of that single entry. In Kelly the buffers that drive the bus are adequate to enqueue a single entry and the process of enqueuing consists of latching the data output from the temporary queues as a result of arbitration into a buffer for driving the bus, an interpretation supported, for example, by Kelly's arbiter multiplexer (e.g., col. 9, lines 56-67). Although a queue may typically have more than one element, in no claim does the recitation support this. To distinguish over Kelly the claimed invention must be appropriately narrowed.

Thus the rejection of claims 1-15, 20-23, 25-30 is maintained.

Regarding the obviousness rejection, Applicant argues incorrect application of teaching reference Shah. As stated supra this argument is persuasive and the previous rejection under 35 USC 103 is withdrawn.

A new ground of rejection is presented for claims 16-19 and 24.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clifford H Knoll whose telephone number is 703-305-8656. The examiner can normally be reached on M-F 0630-1500.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

chk